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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,384	09/17/2003	Victor Roberts Augsburg	RPS920030054US1	4418

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,384	AUGSBURG ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification and Drawings as filed 17 September 2003; Oath and Declaration as filed 17 September 2006; IDS as filed 17 September 2003; and Request for correct filing Receipt as received 25 March 2004.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swanson et al.'s "An Evaluation of Speculative Instruction Execution on Simultaneous Multithreaded Processors" ©August 2003 (herein referred to as Swanson) in view of Teruyama, U.S. Patent Application US2003/0182536 (herein referred to as Teruyama).

5. Referring to claims 1, 8, 16, and 24, taking claim 16 as exemplary, Swanson has taught a simultaneous multithreaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

a. Multiple independent input buffers, wherein one set of buffers is provided for each of a plurality of independent threads of instructions (Swanson page 315, paragraphs 2-3; page 316, paragraph 2; page 319, paragraph 4; page 330,

paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1). In regards to Swanson, the individual buffers for each thread is inherent. Please see Parady, U.S. Patent Number 5,933,627 and Loikkanen and Bagherzadeh's "A Fine-Grain Multithreading Superscalar Architecture" ©1996 for more information.

b. Instruction issue logic that is connected to the independent input buffers (Swanson page 315, paragraphs 2-3; page 316, paragraph 2; page 319, paragraph 4; page 330, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1), wherein the instruction issue logic:

i. Receives instructions from each of the threads of instructions (Swanson page 315, paragraphs 2-3; page 316, paragraph 2; page 319, paragraph 4; page 330, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1);

ii. Determines a confidence factor for each instruction that indicates a probability that the instruction will complete all stages of the multi-stage pipeline without causing a stall (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1); and,

iii. Issues instructions with confidence factors above a predetermined threshold (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

6. Swanson has not taught

i. Predicts a stage, within a multi-stage pipeline of the processor, in which a result from each instruction will be available;

ii. Identifies as dependent instructions those received instructions that require a result from a prerequisite instruction; and

iii. Wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic.

7. Teruyama has taught

i. Predicts a stage, within a multi-stage pipeline of the processor, in which a result from each instruction will be available (Teruyama paragraphs 0011-0014, 0032-0037, and 0082-0083; and Figure 5);

ii. Identifies as dependent instructions those received instructions that require a result from a prerequisite instruction (Teruyama paragraphs 0011-0014, 0032-0037, and 0082-0083; and Figure 5); and

iii. Wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic (Teruyama paragraphs 0011-0014, 0032-0037, and 0082-0083; and Figure 5).

8. A person of ordinary skill in the art at the time the invention was made, and as taught by Teruyama, would have recognized that tracking the dependencies of an instruction ensures that instructions without dependencies are not cancelled inappropriately that results in reduced efficiency and speed (Teruyama paragraph 0013), thereby improving efficiency and speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to incorporate the dependency tracker of Teruyama in the device of Swanson to improve processor efficiency and speed.

9. Claims 1, 8, and 24 are functionally equivalent to claim 16 and are rejected for similar reasons. Claim 1 differs only in that it is a method claim. Claims 8 and 24 differ in that they are for a single threaded system. Swanson states on page 315, paragraph 2 that a simultaneous multithreading system can execute one thread and that all resources are dedicated to that thread, meaning that an SMT system can be a single threaded system with all buffers containing instructions for that thread.

10. Referring to claims 2, 9, 17, and 25, taking claim 17 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 16, wherein the instruction issue logic stores the predicted pipeline stage for each instruction (Teruyama paragraphs 0011-0014, 0032-0037, and 0082-0083; and Figure 5) and, dynamically updates the stored predicted pipeline stage for each instruction based on a current contents of the pipeline (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

11. Referring to claims 3, 10, 18, and 26, taking claim 18 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 16, wherein the confidence factor for an instruction is determined based upon a current location and the predicted stage of the prerequisite instruction (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

12. Referring to claims 4, 11, 19, and 27, taking claim 19 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 17, wherein the instruction issue logic

dynamically recalculates the confidence factor for each instruction based on the current contents of the pipeline (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

13. Referring to claims 5, 12, 21, and 28, taking claim 21 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 16, wherein the instruction issue logic further identifies as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates (Teruyama paragraphs 0011-0014, 0032-0037, and 0082-0083; and Figure 5).

14. Referring to claims 6, 13, 22, and 29, taking claim 22 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 21, wherein the confidence factor for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

15. Referring to claims 7, 14, 23, and 30, taking claim 23 as exemplary, Swanson in view of Teruyama has taught the computer processor of claims 22, wherein the instruction issue logic dynamically recalculates the confidence factor for each instruction based on a current contents of the pipeline and a current status of any shared resources (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

16. Referring to claims 15 and 20, taking claim 20 as exemplary, Swanson in view of Teruyama has taught the computer processor of claim 16, wherein one or more instruction(s)

is(are) issued from the instruction issue logic every clock cycle (Swanson page 317, paragraph 1; page 326, paragraphs 4-7; page 327, paragraph 1 to page 328, paragraph 1; and page 336, paragraph 4 to page 337, paragraph 1).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Martin Brutscher and Benjamin G. Zorn's "Prediction Outcome History-based Confidence Estimation for Load Value Prediction" ©1999 has taught prediction using confidence value.

b. Arora, U.S. Patent Number 6,442,678, has taught speculative execution where different instructions produce speculative results at different stages in the pipeline and the speculative results are available for other instruction use one clock cycle after the speculative results are available.

c. Teruyama, U.S. Patent Number 6,601,162, has taught a system with speculative execution and result bypassing.

d. Bittel et al., U.S. Patent Number 6,820,173, has taught a prediction system using confidence values.

e. Parady, U.S. Patent Number 6,907,520, has taught a multi-threaded system with speculative execution using confidence values.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER

AJL
Aimee J. Li
23 June 2006